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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 09/22/2004

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/22/04, 8/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

1. Claims 1-18 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/3/04 has been entered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orton et al. (Orton), US patent no. 6,118,306, in view of "Re: AX64Pro or AK72?", NewsReader, June 15, 2000, pages 1-2; (hereinafter, "Newsreader").

Orton is a prior art reference cited by applicant in IDS paper no. 6.

As per claim 1, Orton teaches a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 2, lines 44-60]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable [col. 3, lines 10-20].

Orton does not explicitly teach that the value of the core voltage is not sufficient to maintain processing activity in said processor. In other words, Orton does not teach reducing the core voltage to one Volt or less during deep sleep mode.

Newsreader teaches of reducing the core voltage to one Volt or less during deep sleep mode [page 2, paragraph 3]. Therefore, Newsreader teaches that the value of the core voltage is not sufficient to maintain processing activity in said processor.

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and Newsreader because they are both directed to the problem of reducing the power consumption of a processor core, and the specify teachings of Newsreader stated above would improve power consumption by further reducing the core voltage to a minimum supported voltage.

As per claim 2, Orton teaches of determining the processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal [col. 2, lines 44-60; col. 5, lines 4-11; col. 7, lines 38-43].

As per claim 3, Orton teaches of reducing an output voltage providing by a voltage regulator furnishing core voltage to the processor and providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

6. Claims 4, 12 and 14-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Orton et al. (Orton), US patent no. 6,118,306 in view of Applicant Admitted Prior Art (AAPA).

7. As per claim 4, Orton teaches that a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable by [col. 3, lines 10-20]:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58]; and

providing a control signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 2, lines 24-27; col. 3, lines 10-19; col. 7, lines 14-19, 44-58].

Orton does not explicitly teach of providing a feedback to the voltage regulator.

AAPA teaches of providing a feedback to the voltage regulator [page 5, lines 6-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 18, Orton teaches that the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to furnishing the input to reduce the output voltage provided by the voltage regulator [col. 7, lines 14-58].

8. As per claim 12, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings", inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 7, lines 50-65].

Orton does not explicitly disclose a voltage regulator feedback circuit and a voltage divider network.

AAPA discloses a voltage regulator including a voltage regulator feedback circuit and a voltage divider network [page 5, lines 6-9].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

9. As per claim 14, is contained same limitations as set forth in claim 12. Therefore, same rejection is applied.

As per claim 15, Orton teaches that the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode [col. 7, lines 50-65].

As to claims 16 and 17, AAPA discloses that the feedback circuit comprises a voltage divider [page 5, lines 6-9].

10. Claims 5-11 and 13 are rejected under 35 U.S.C. 102 (a) or 102(e) as being anticipated by Orton et al. (Orton), US patent no. 6,118,306.

As per claim 5, Orton teaches a method for reducing power utilized by a processor comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 44-60];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable; [col. 3, lines 10-20]; and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined at a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 2, lines 11-27, 44-65; col. 7, line 59-col. 8, line 5].

As per claim 6, Orton teaches of returning the voltage regulator to its original mode of operation [col. 3, lines 10-14; col. 7, lines 51-58; col. 8, lines 54-65].

11. As per claim 7, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65], wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor [col. 2, lines 44-65; col. 3, lines 10-20; col. 7, line 59-col. 8, line 5].

As per claim 8, Orton discloses that the voltage regulator comprises means for accepting binary signals [LO/HI signals] indicating different voltage level [fig. 5; col. 7, lines 20-37, 63-65; "A signal **VR_LO/HI#**...adjust the voltage level supplied by the voltage regulator 52 up or down"].

As per claim 9, Orton discloses that the voltage regulator comprises:

Selection circuitry, means for furnishing a plurality of signals at the input to the selection circuitry and means for controlling the selection by the selection circuitry [fig. 3A] [col. 5, lines 38-55].

As per claim 10, Orton discloses a multiplexor [col. 5, lines 44-45; fig. 3A] and means for controlling the selection by the selection circuitry including a control terminal for receiving signals indicating a system clock to the processor is being terminated [col. 5, lines 38-65].

12. As per claim 11, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines 28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 7, lines 50-65].

13. As per claim 13, Orton discloses a circuit [fig. 5] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, fig. 1, fig. 5] having: an output terminal [col. 7, lines 50-51; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 10-12; col. 7, lines

28-31, 46-47, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 5; col. 7, lines 52-55; "the voltage interface provided the control logic portion 400 allows the voltage regulator 52 to change settings" , inherently, there is an input terminal in the voltage regulator 52] for receiving signals indicating the selectable voltage level;

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 7, lines 50-65],

circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 7, lines 28-58].

14. Applicant's argument with respect to claims 1-13 have been considered but is moot in view of the new ground(s) of rejection.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

AMD Athlon; "Processor Module" datasheet, discloses a table of core voltage operating ranges for a processor module [page 28, table 8].

Intel, "Pentium III Processor for the SC242 at 450 MHz to 866 MHz and 1.0 GHz", Datasheet, teaches of a processor is incapable of responding to snoop transactions or latching interrupt signals in deep sleep state [page 16, paragraph 2.2.6].

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106 (571-272-3664, effective 10/14/2004). The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717 (571-272-3667, effective 10/14/2004). The fax number for this Art Unit is following: Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631 (571-272-2100, effective 10/14/2004).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Sep. 17, 2004